# A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 layers of Cu Interconnects, Low k ILD, and 1 $um^2$ SRAM Cell

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Logic Technology Development, * TCAD, # QRE

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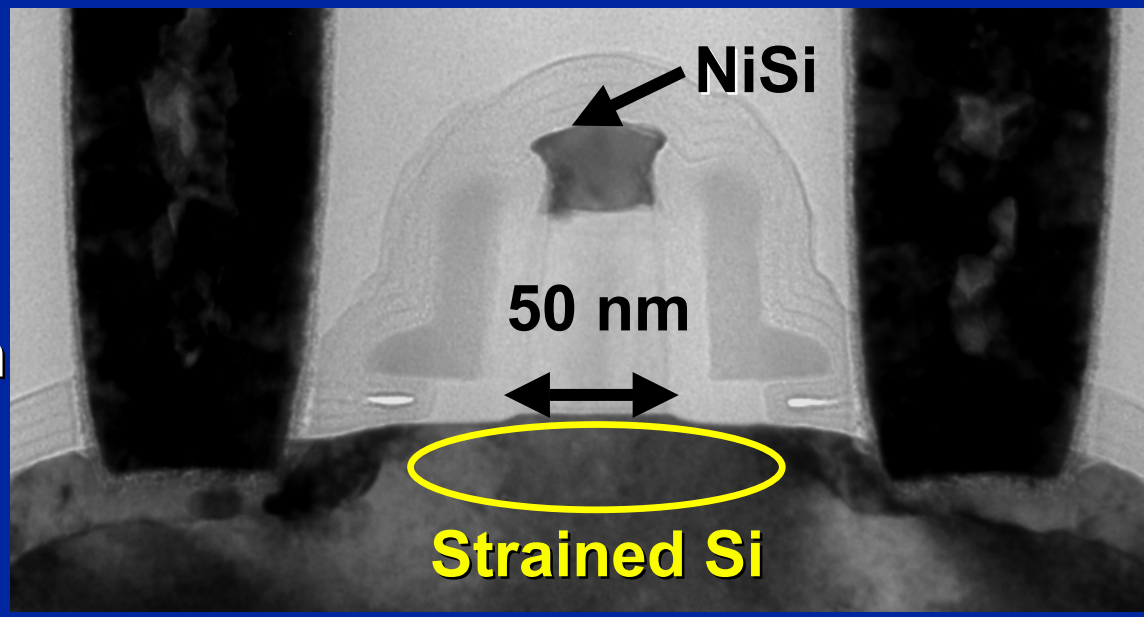
# Outline

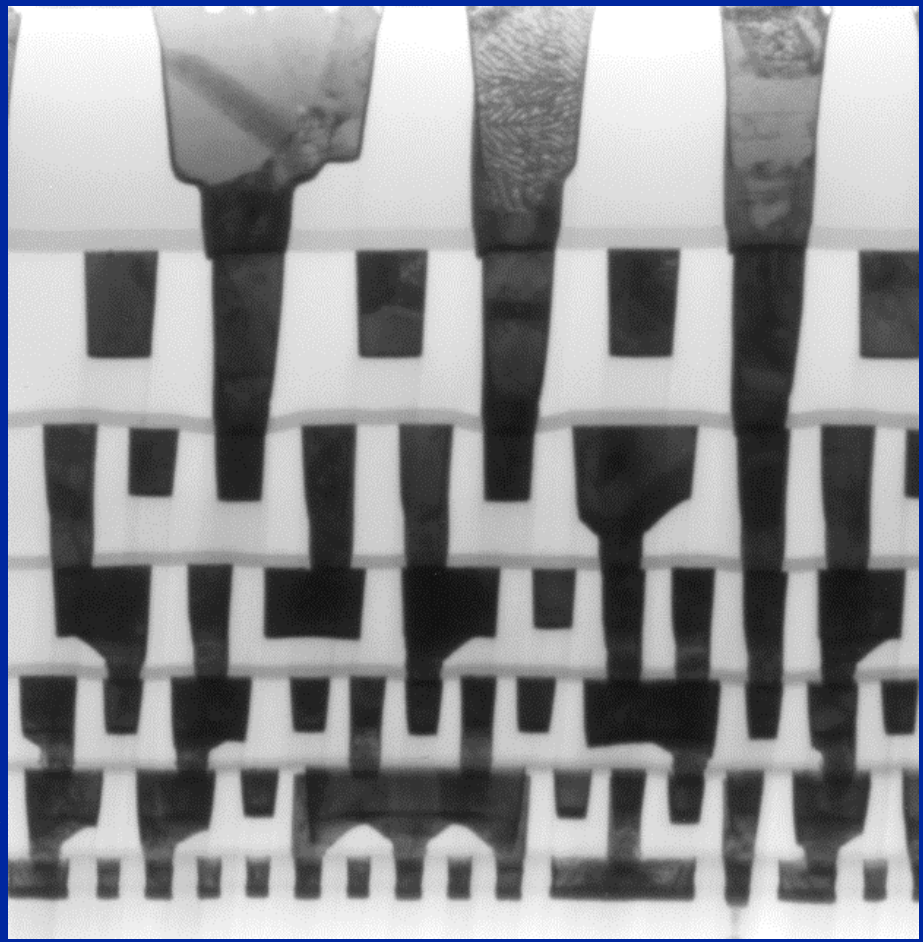
- Process Flow and Technology Features
- Transistor Features
- Cu and low K ILD
- 52Mbit SRAM Performance
- Conclusions

# Front End Technology Features

- 193nm litho for critical layers
- 240nm STI pitch
- 1.2nm gate oxide
- 50nm $L_{GATE}$
- Single gate orientation
- Strained-Si
- Ni salicide
- SRAM/Logic use of unlanded contacts



# Back End Technology Features



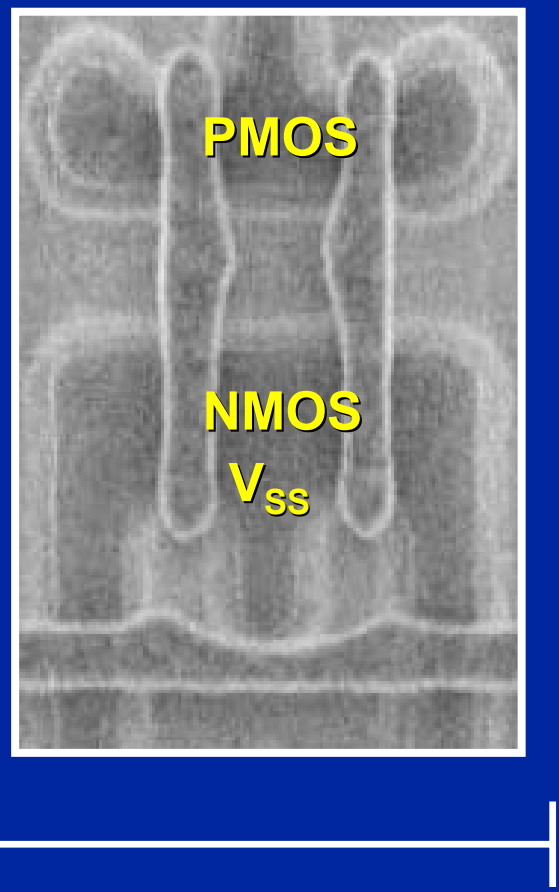
# Pitches and Thicknesses

| LAYER | PITCH | THICK | AR |
|---|---|---|---|
| Isolation | 240 | 400 | - |
| Poly-Si | 260 | 140 | - |
| Metal 1 | 220 | 150 | 1.4 |
| Metal 2,3 | 320 | 256 | 1.6 |
| Metal 4 | 400 | 320 | 1.6 |
| Metal 5 | 480 | 384 | 1.6 |
| Metal 6 | 720 | 576 | 1.6 |
| Metal 7 | 1080 | 972 | 1.8 |

( nm )

# 6-T SRAM Cell

- 1.0 $\mu m^2$ 6-T SRAM cell
- Few array-specific design rules
- SRAM supports operation from 0.75 to 1.2 V



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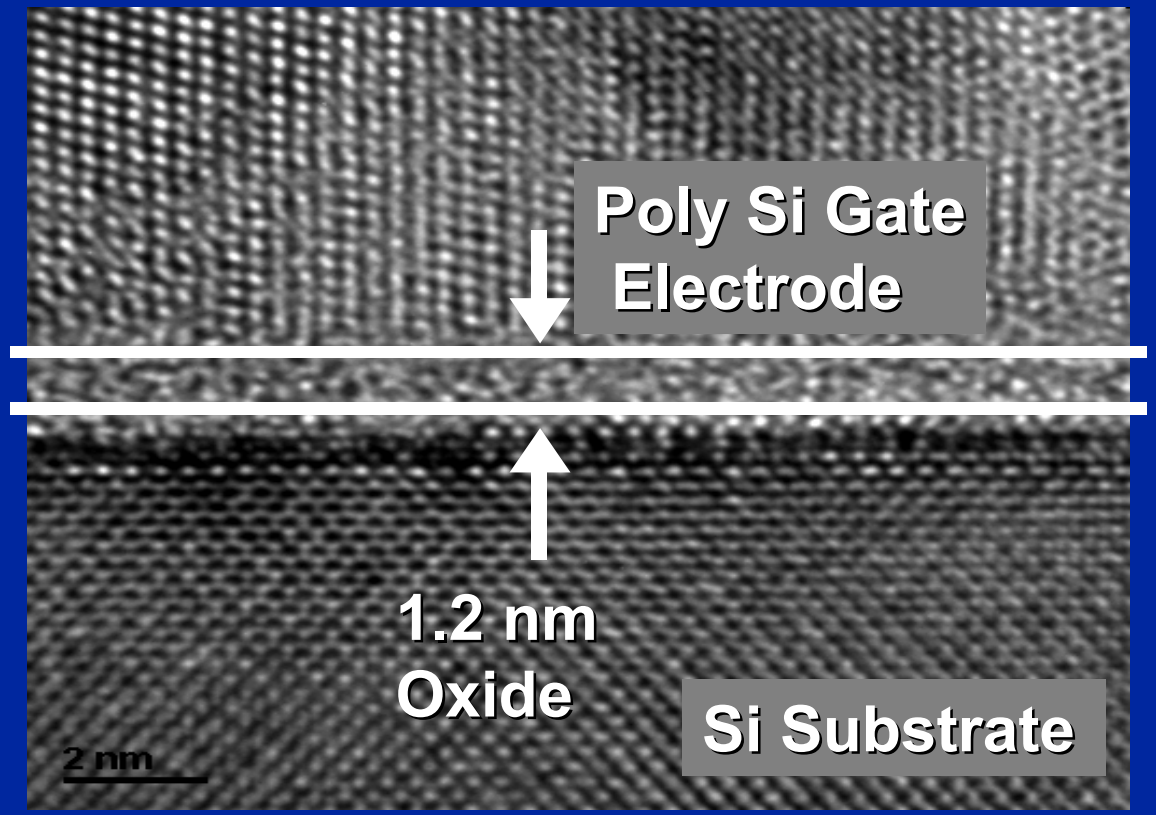
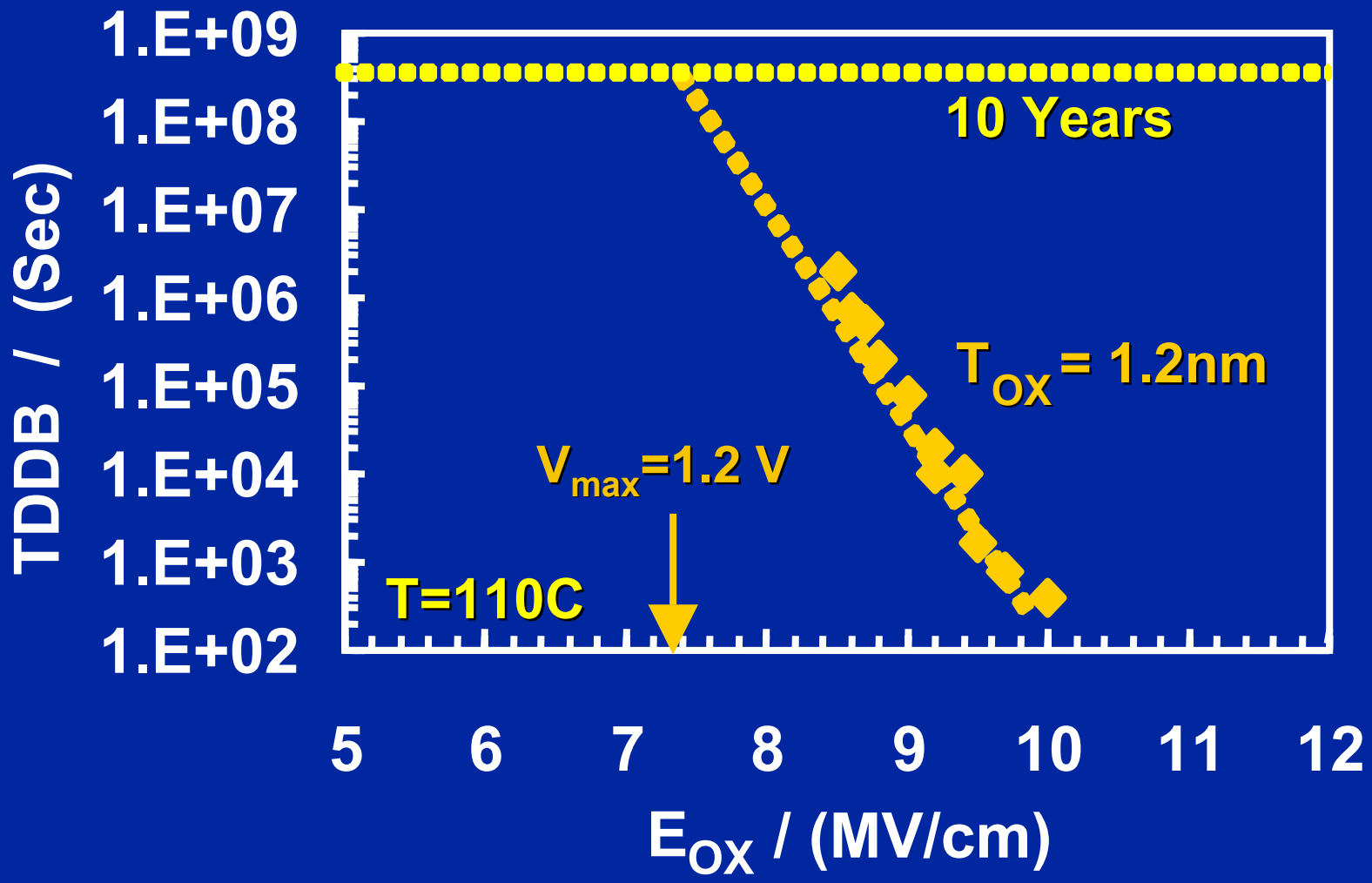
# 1.2 nm Physical Gate Oxide



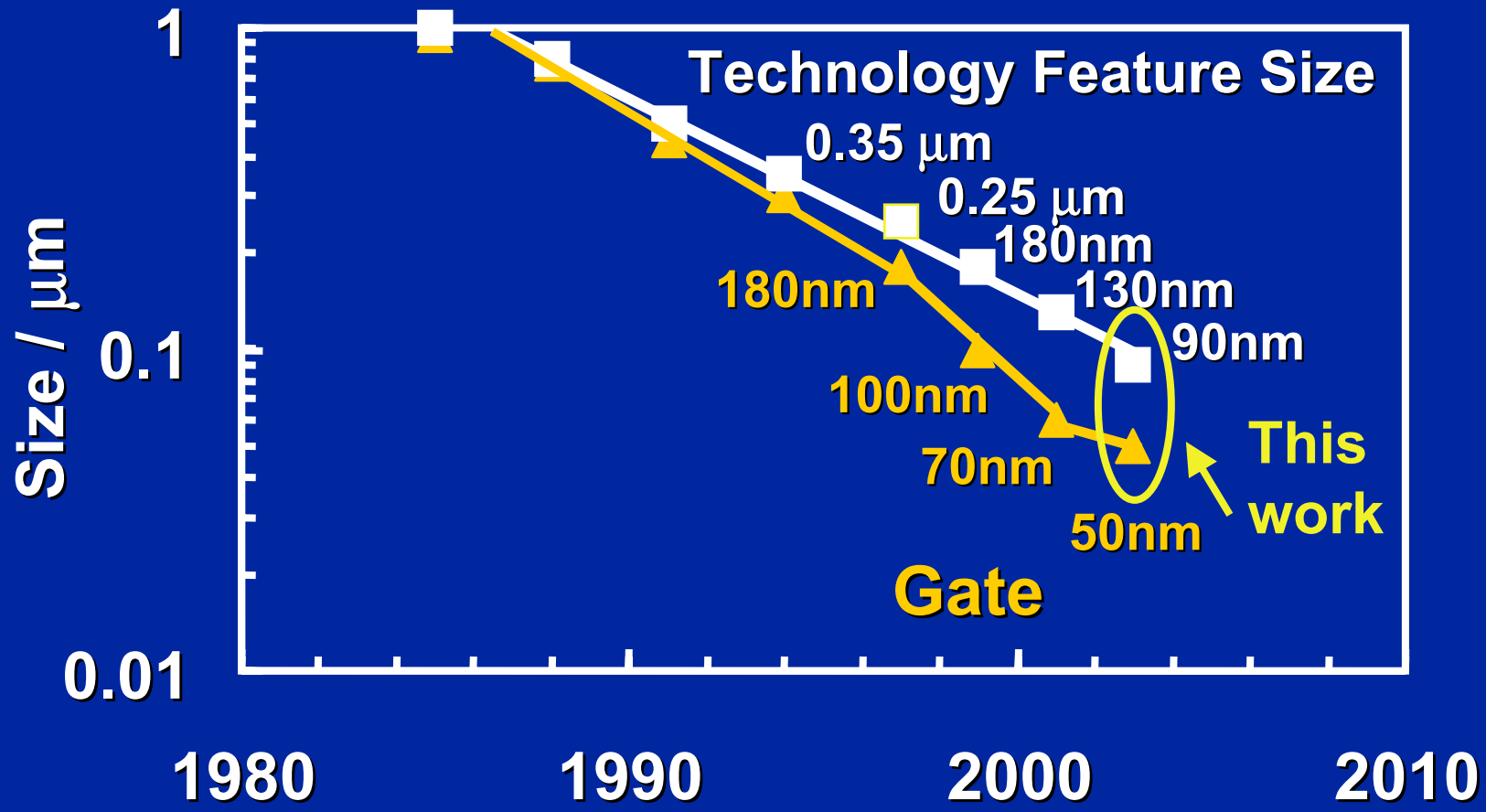

1.2 nm physical gate oxide → ONLY 5 Atomic Layers

# Gate Oxide Reliability

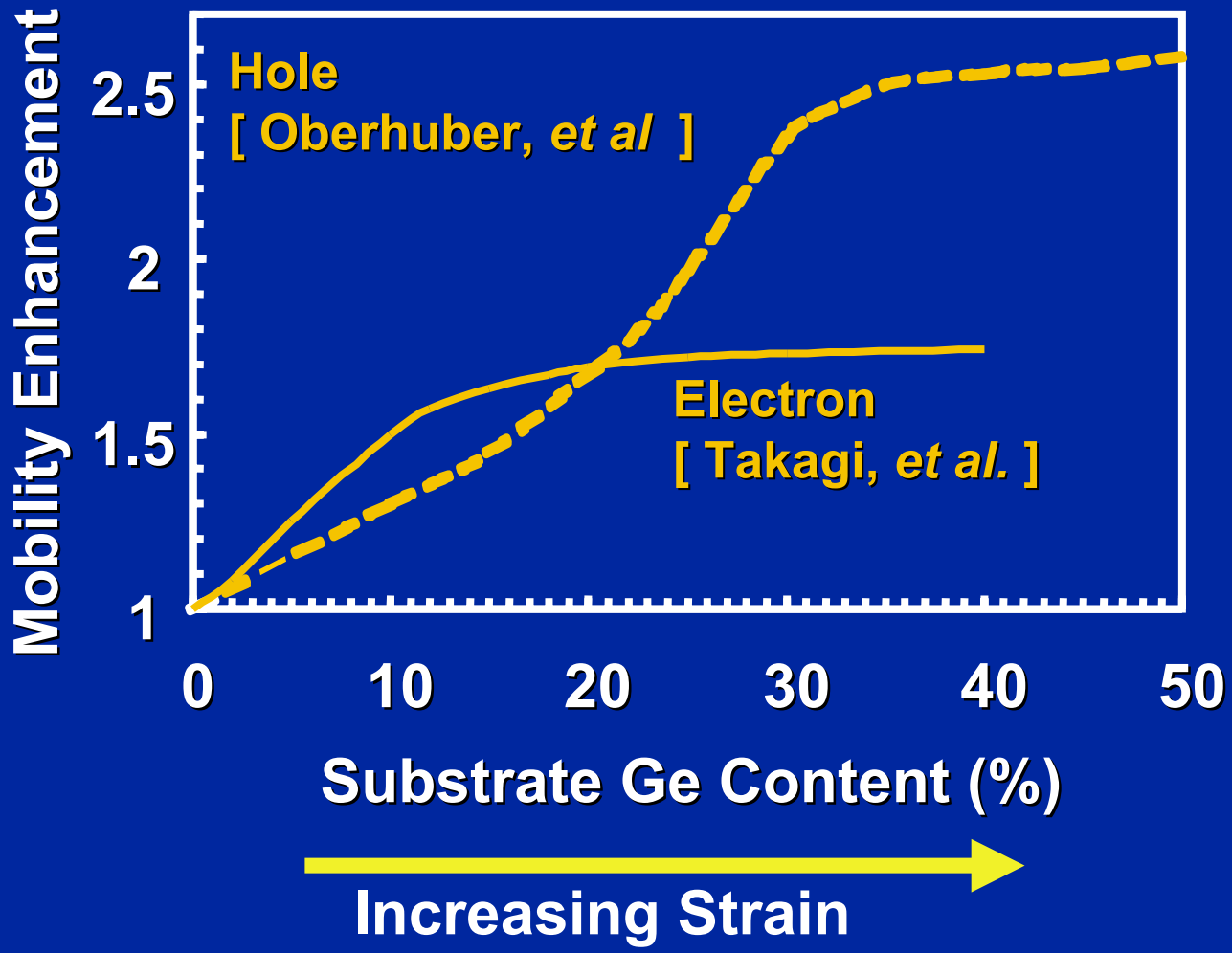


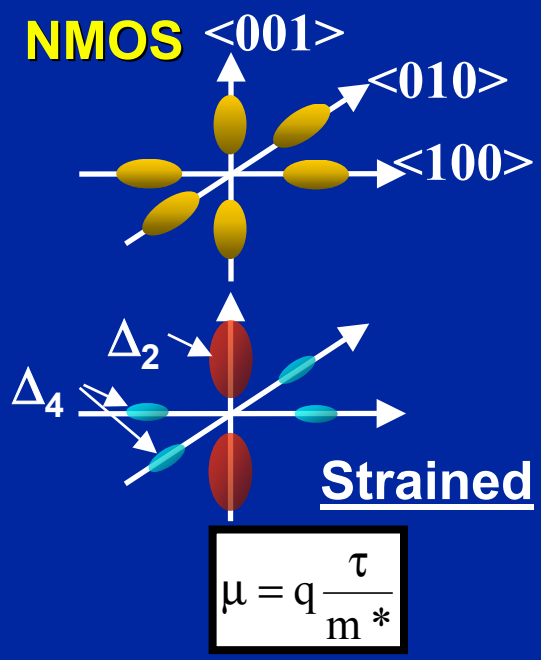

**Exceeds 1.2 V Reliability Criteria**

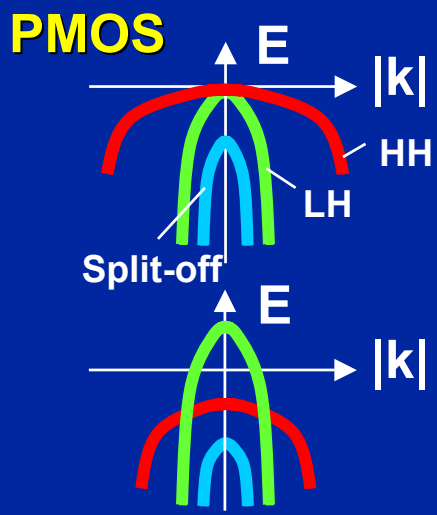
# Gate Dimension Trend



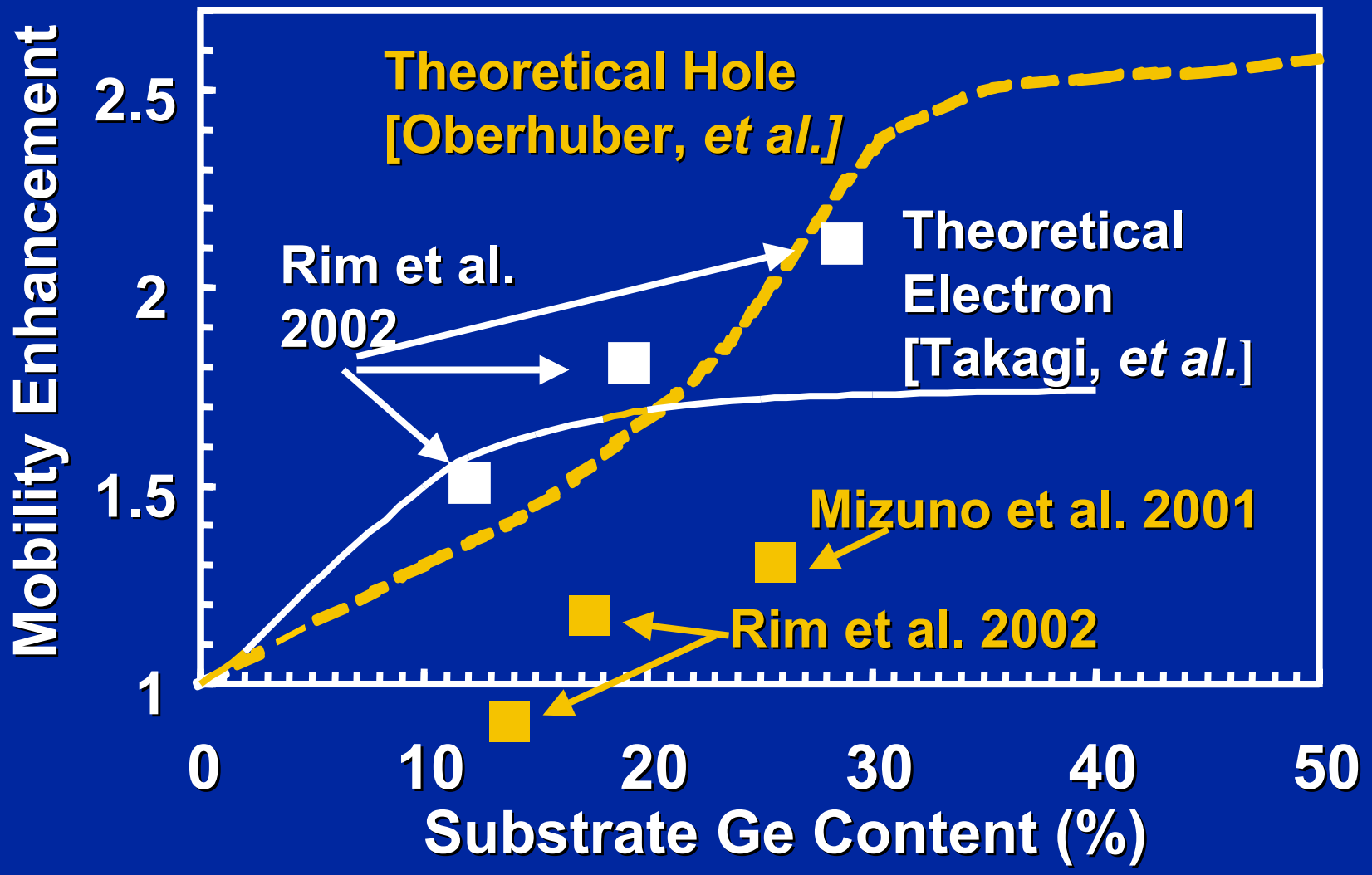
# Strained Silicon Channel Enhances Moore's Law



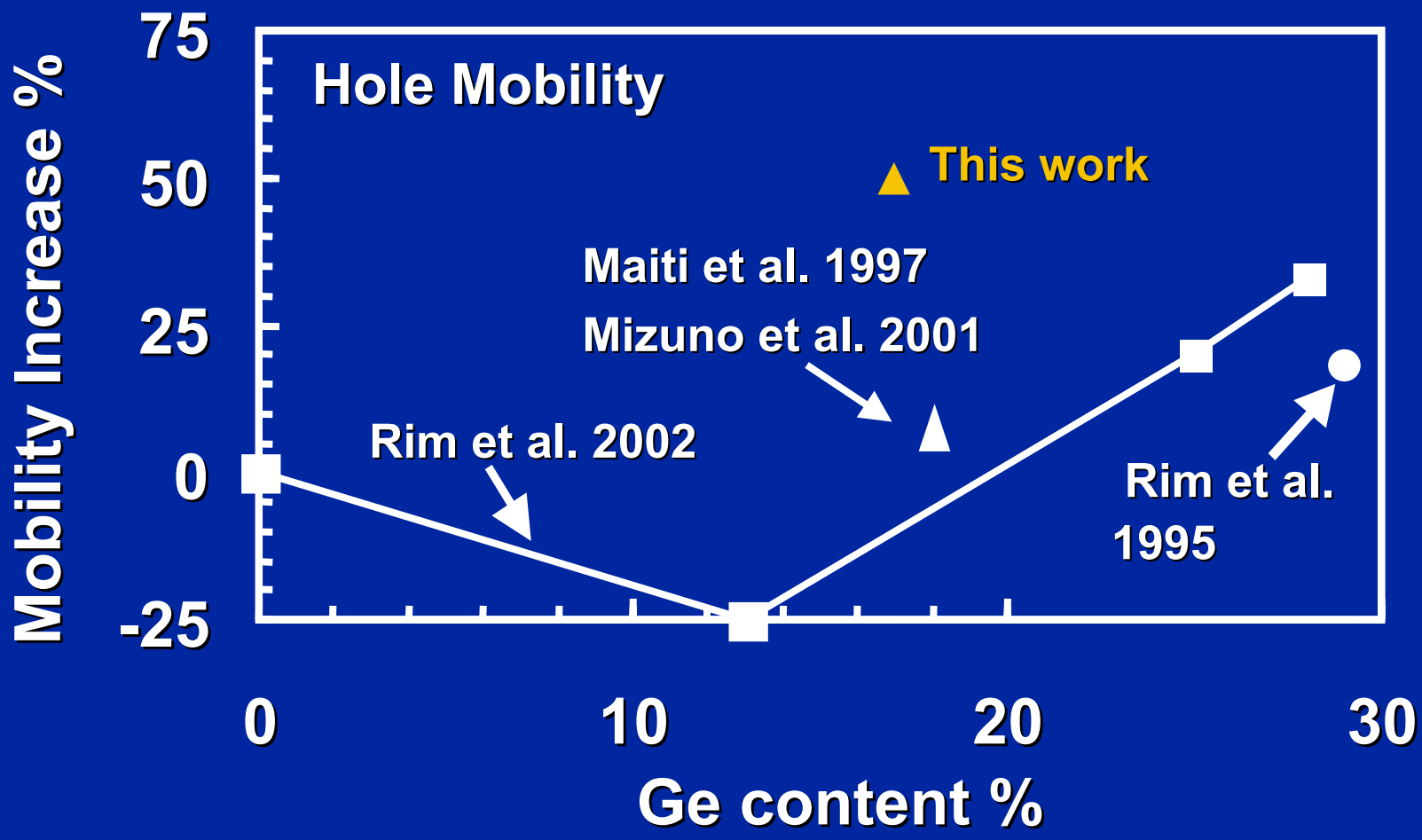



# Experimental vs. Theoretical

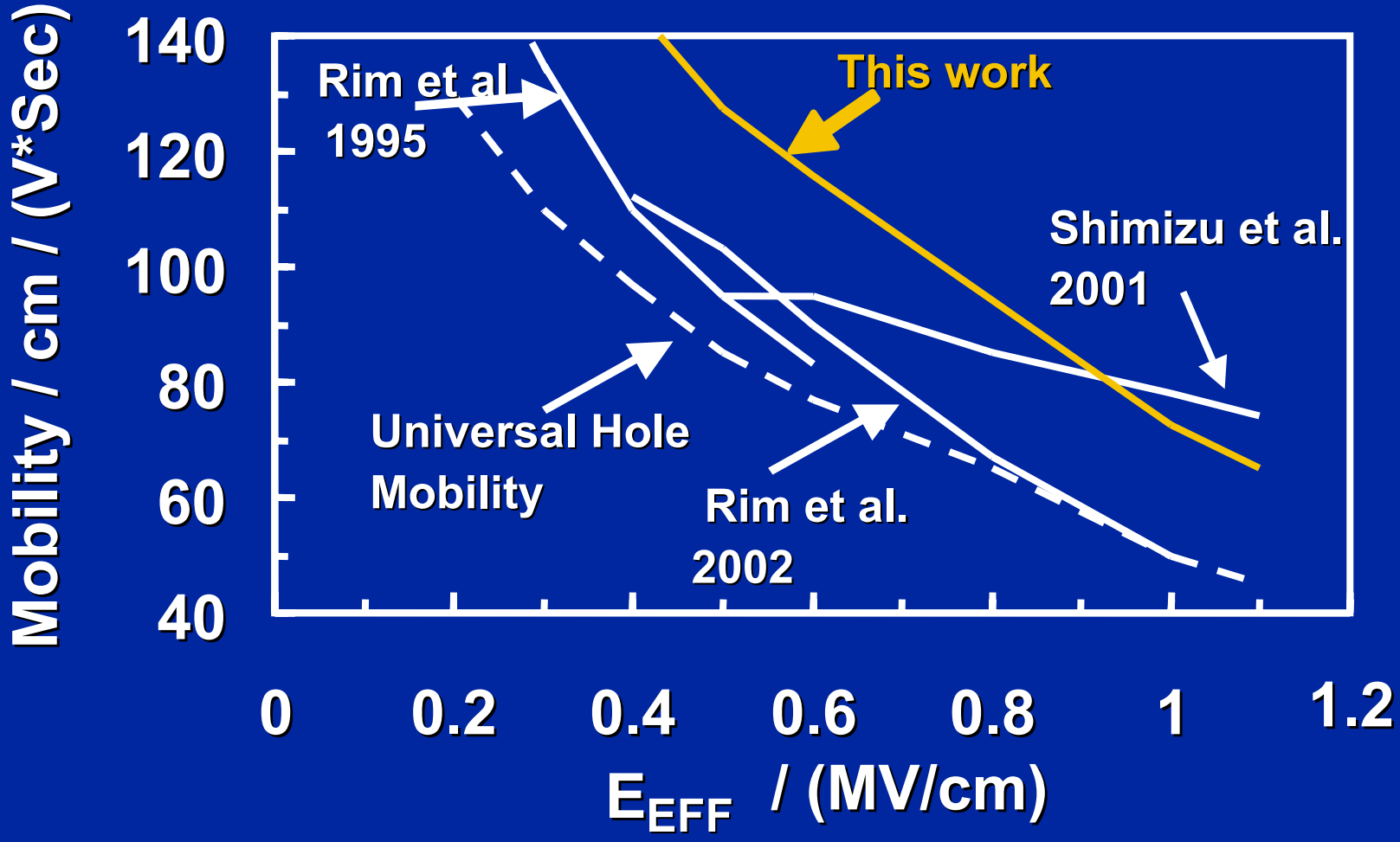



Electron matches, past hole data does not

# Mobility Increase Improvement

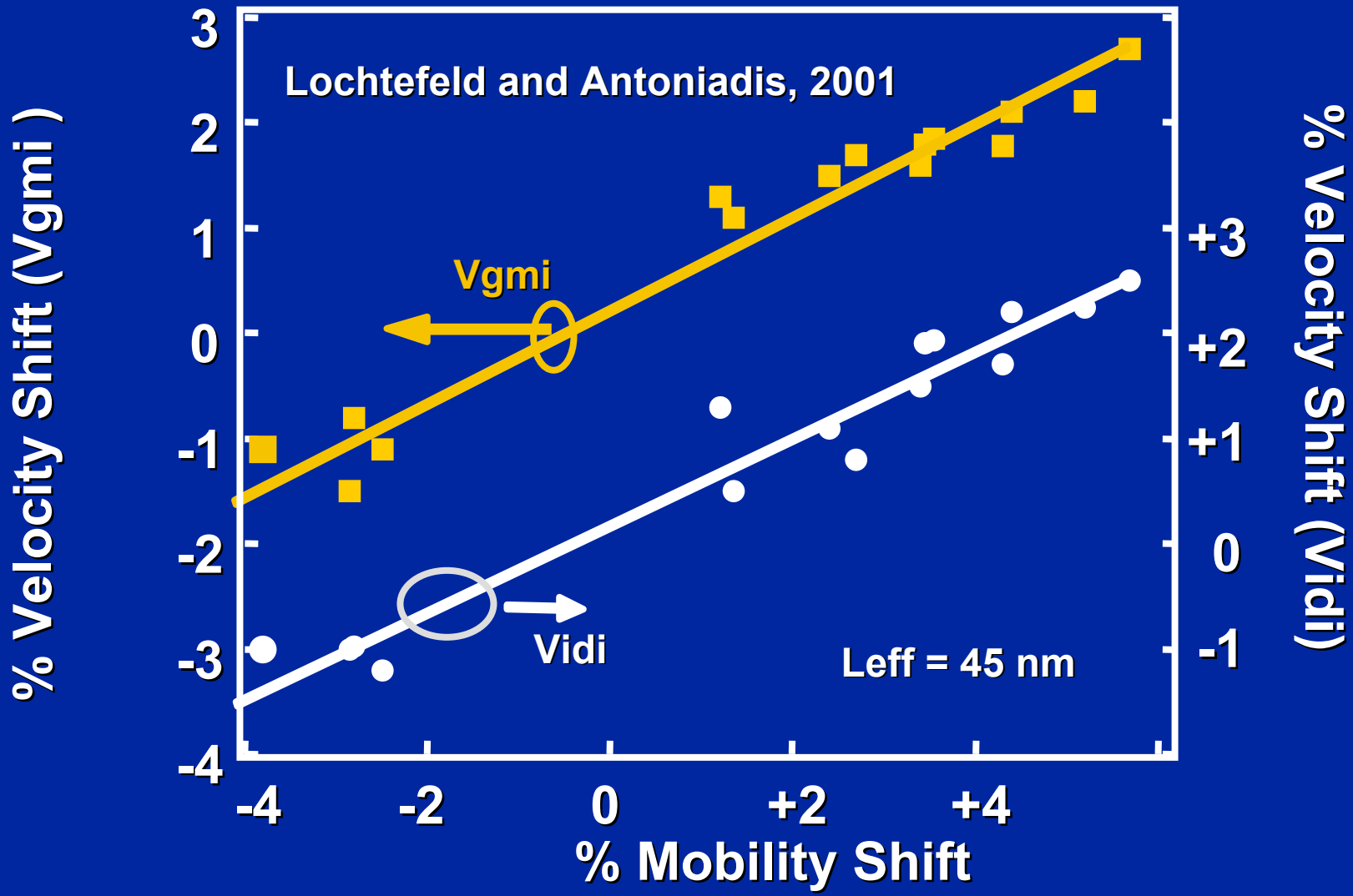


# Hole Mobility Vs. Electric Field



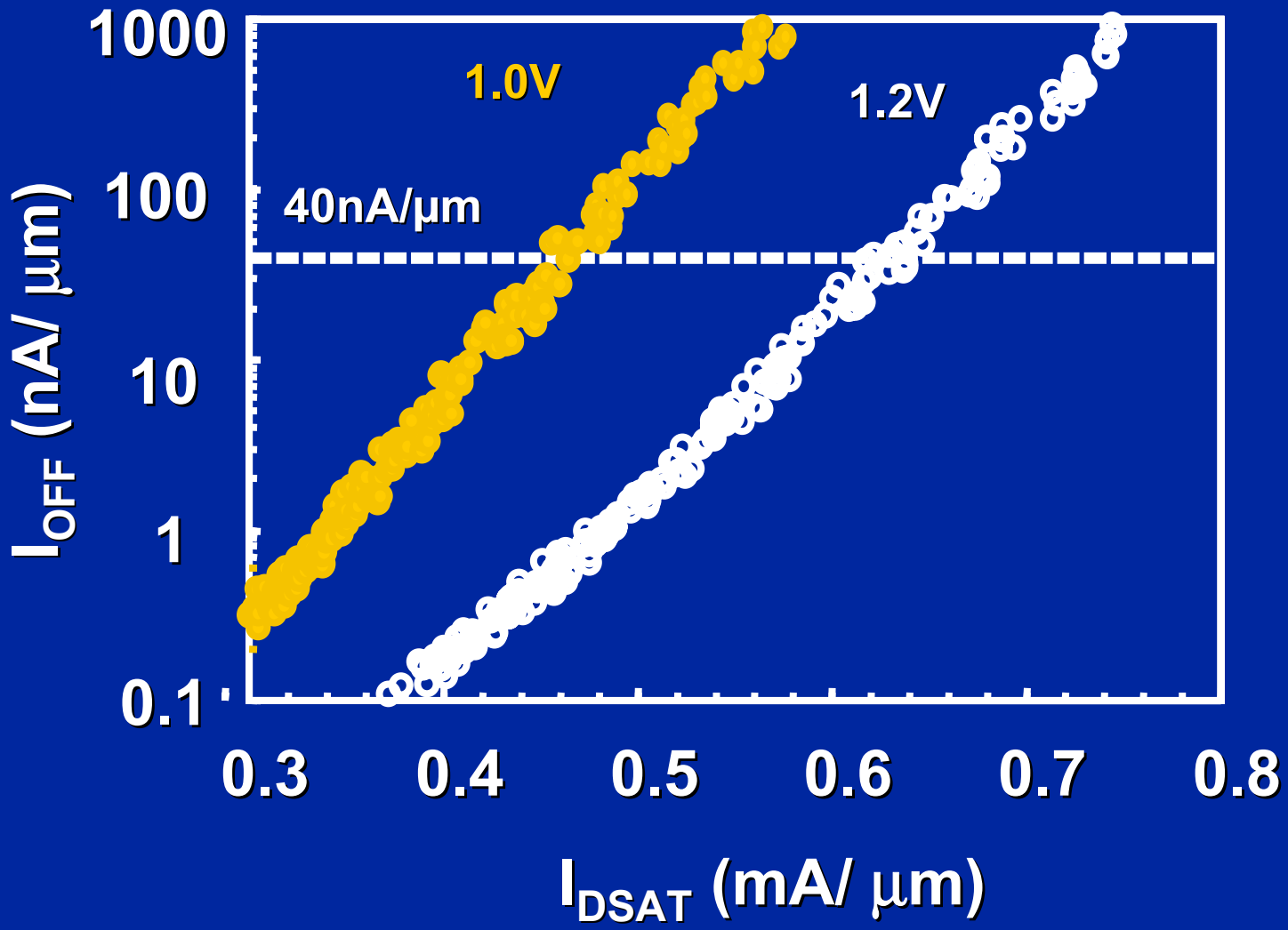

**Improvement maintained over all vertical E-Fields**

# Mobility On Device Performance

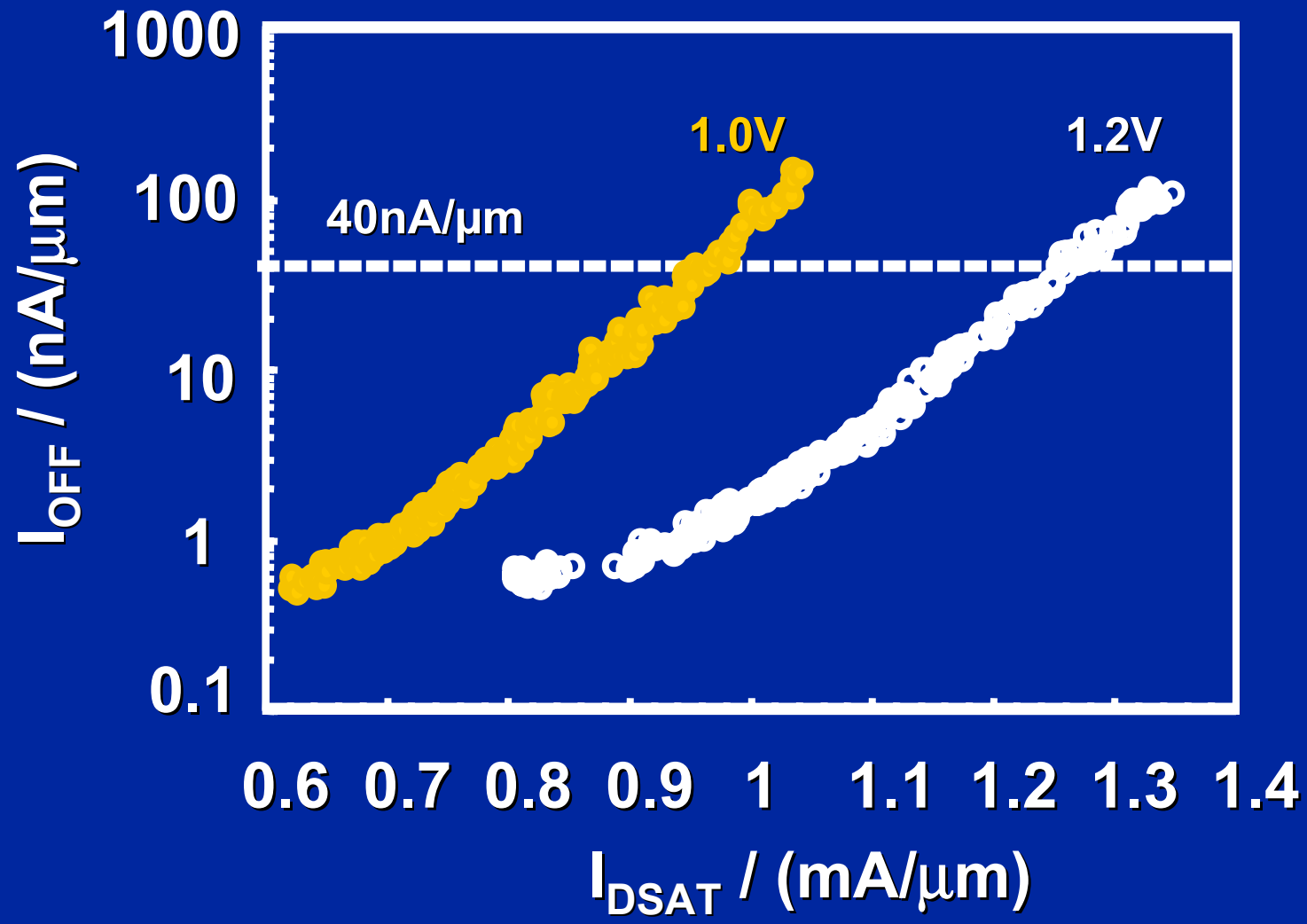



**Strain-enhanced mobility improves $I_{DSAT}$ for <0.1μm devices ( Rim 1998, Lochtefeld 2001)**

# PMOS $I_{DSAT}$ vs $I_{OFF}$



# NMOS $I_{DSAT}$ vs $I_{OFF}$

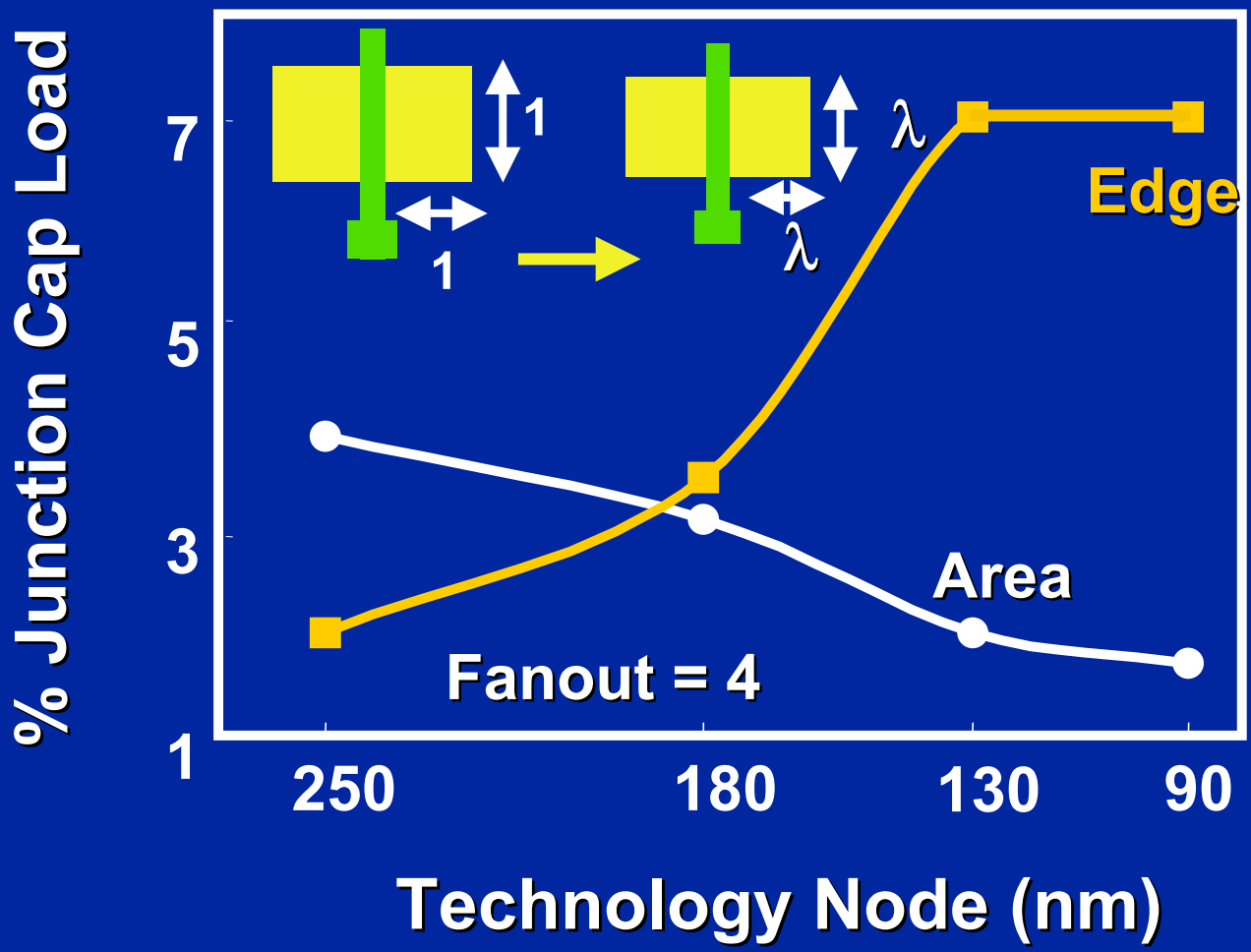


# Junction Capacitance: Edge Dominant Over Area

- Importance of area reduces with scaling
- Area scales as $\lambda^2$ while edge as $\lambda$
- Edge values

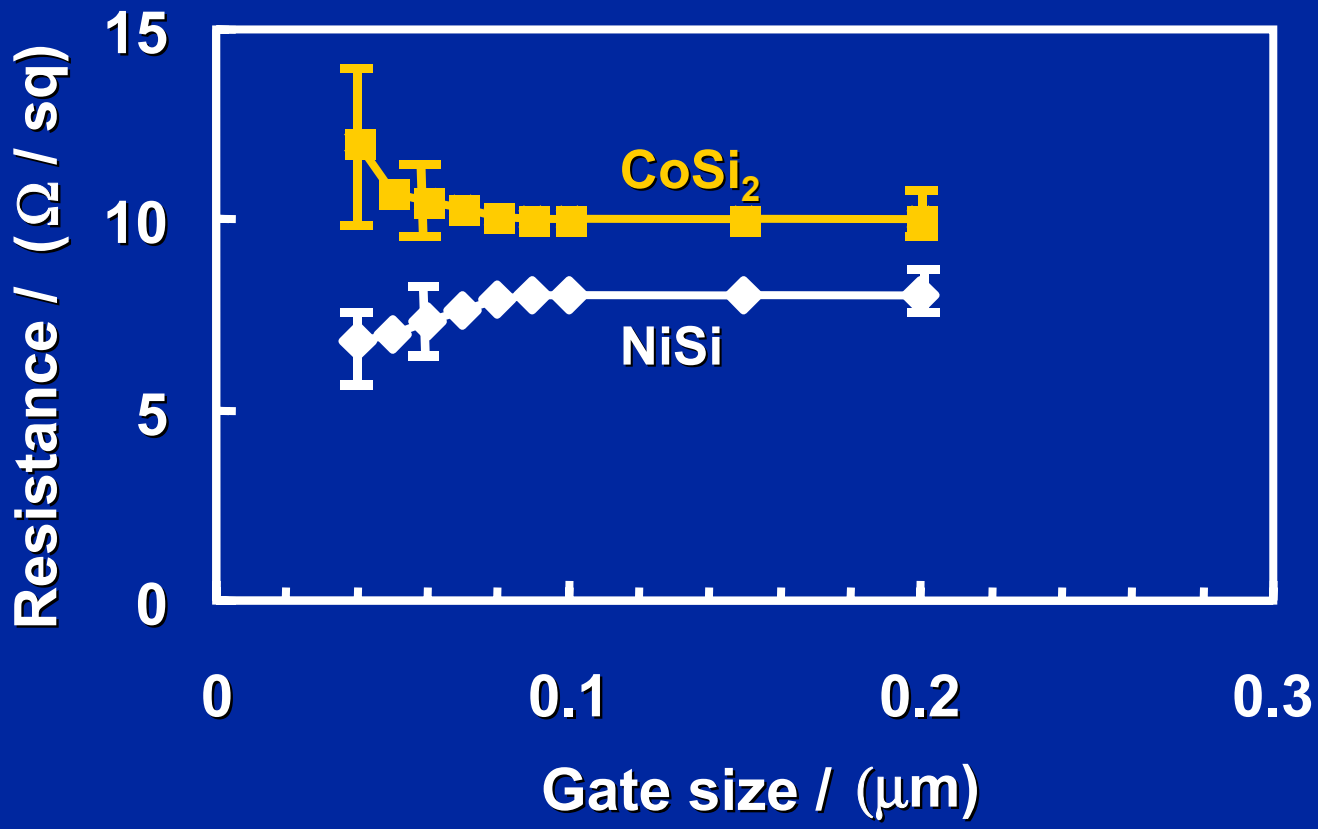
  P = .36fF/μm

  N = .31fF/μm



# NiSi or $CoSi_2$ with Sacrificial Epitaxial Silicon

- Better narrow-line scaling properties
- Lower contact resistance
- Compatibility with SiGe



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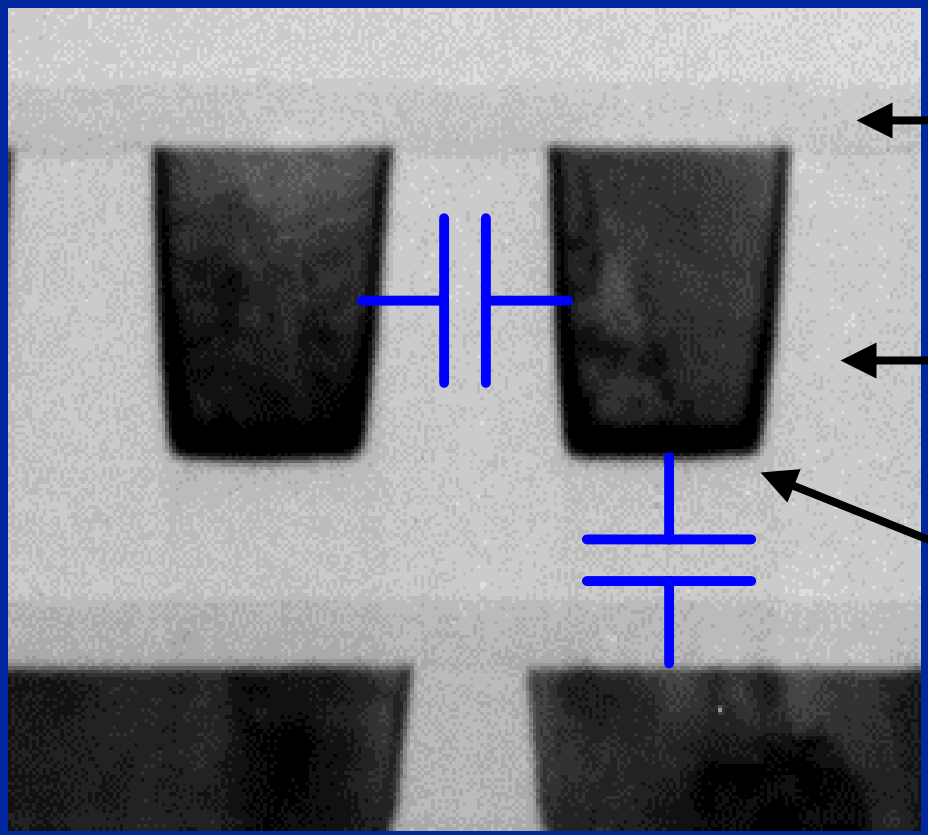
# Interconnect Architecture

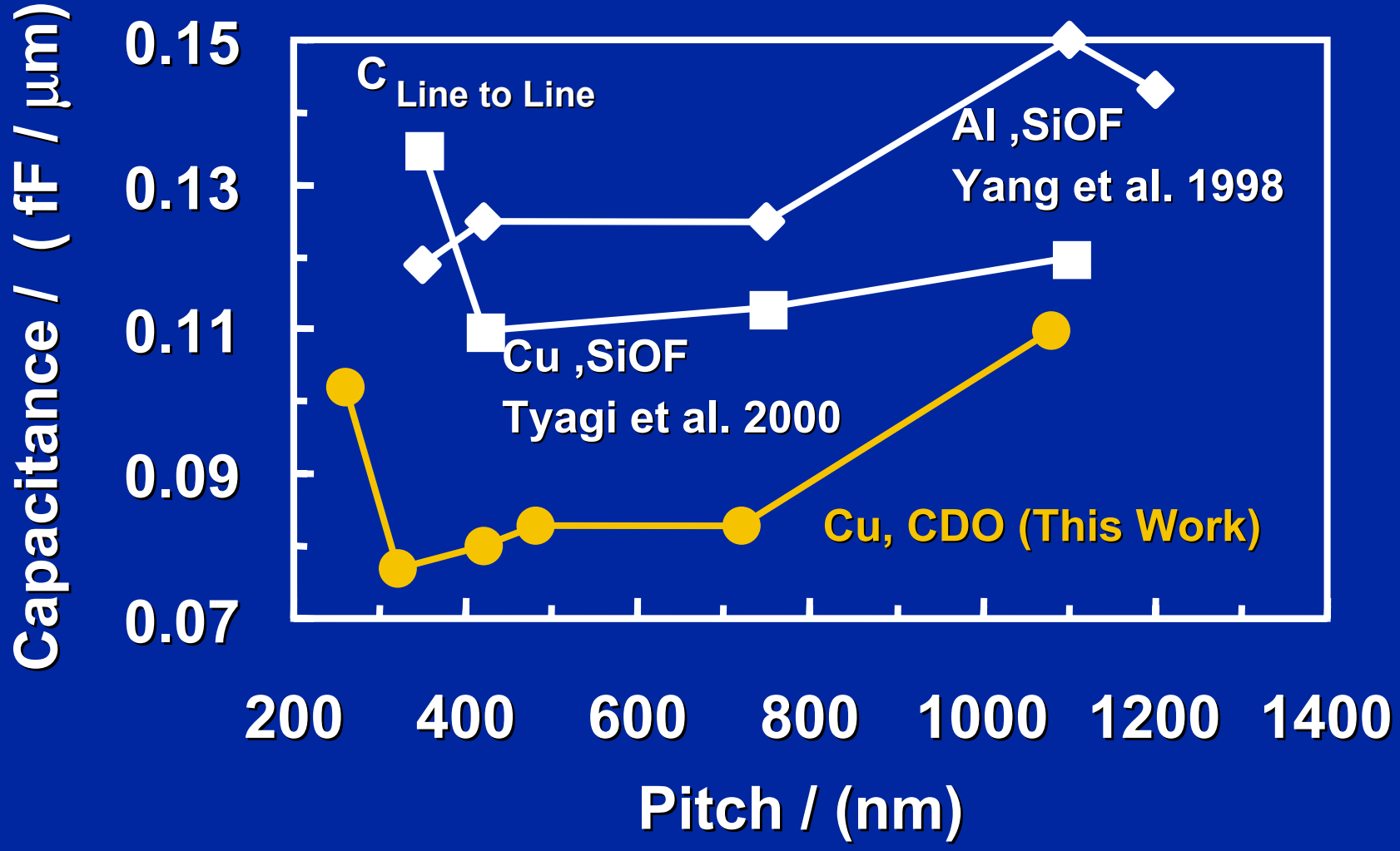


Thin SiN: ($C_X$) layer

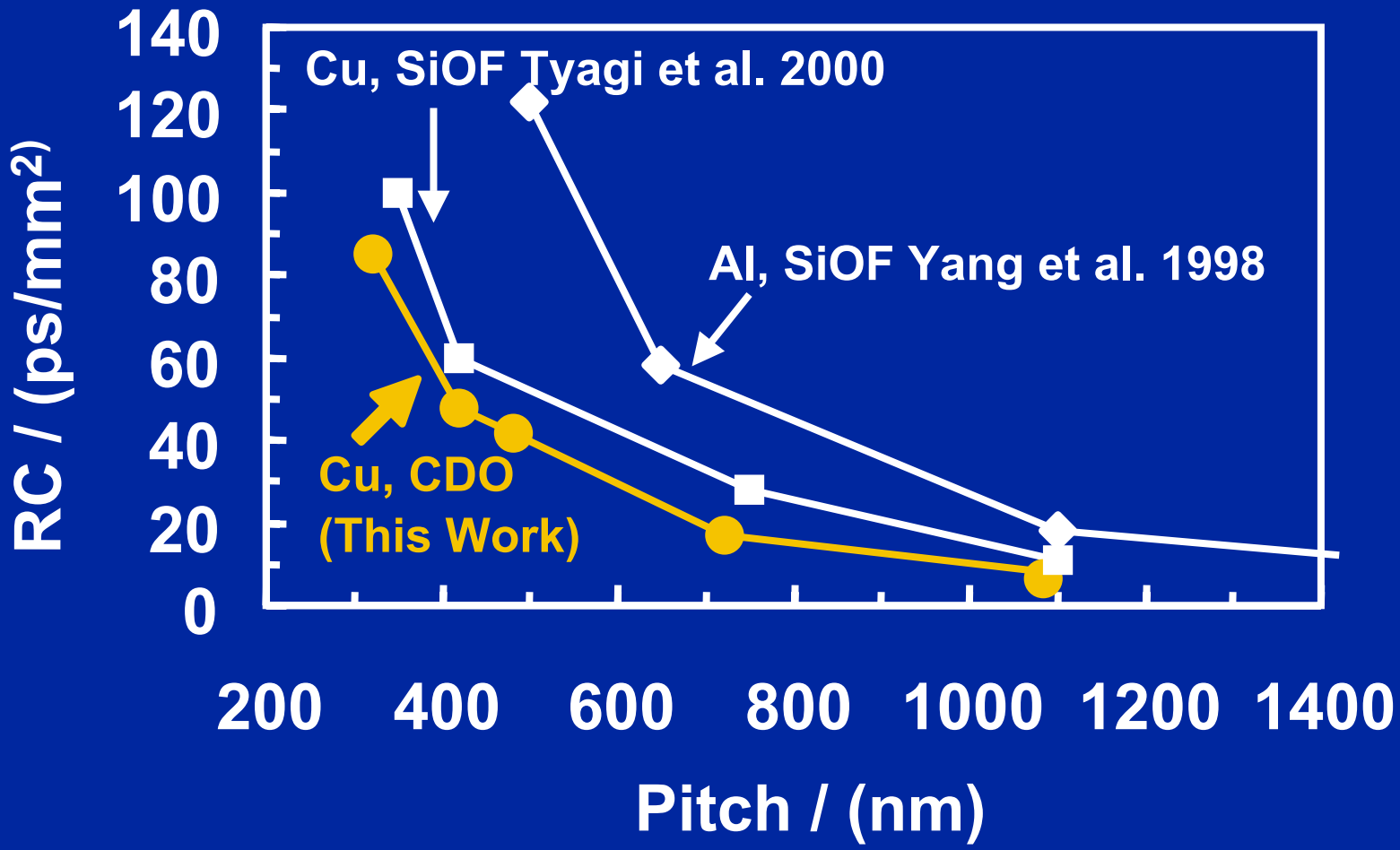
CDO K = 2.9

NO metal etch stop layer

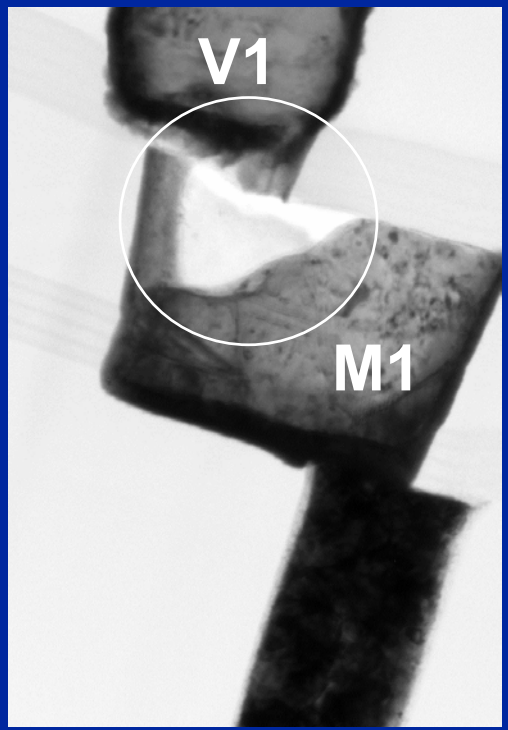
# Line to Line Capacitance



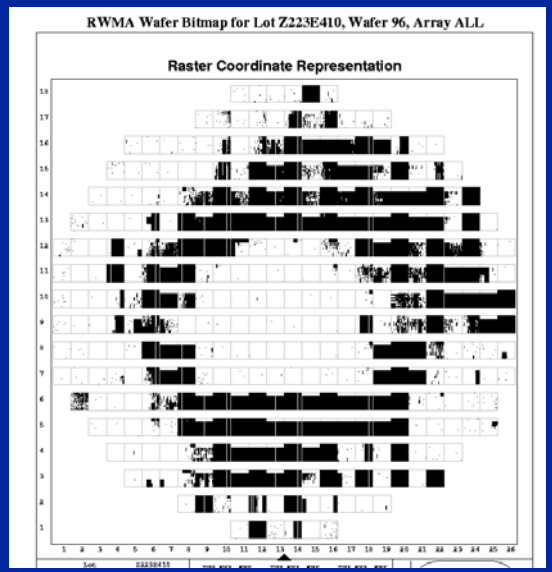
# Backend RC Delay



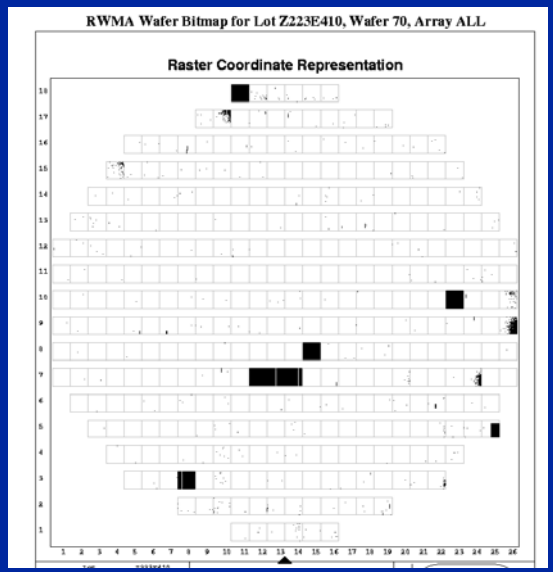
# Void-Free Required for Electromigration




## Old Process

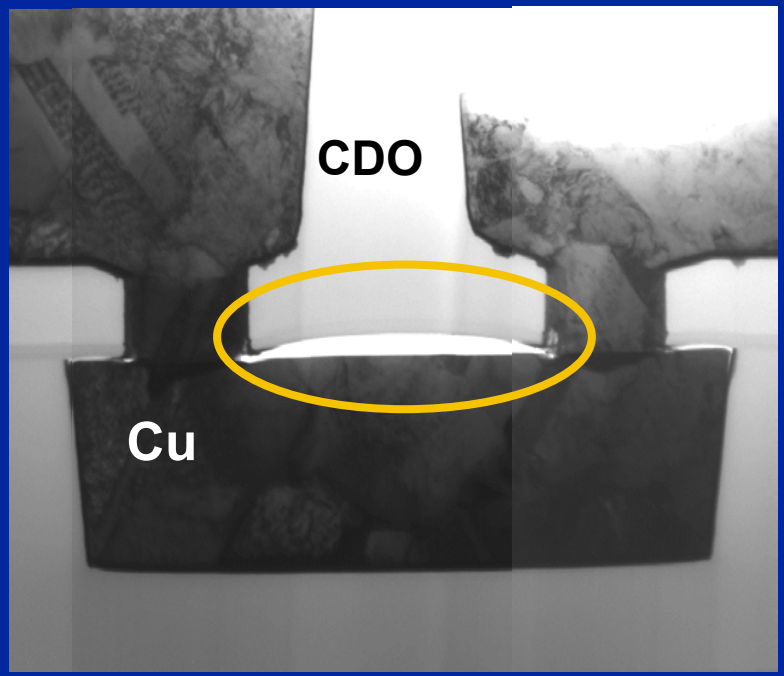



## New Process

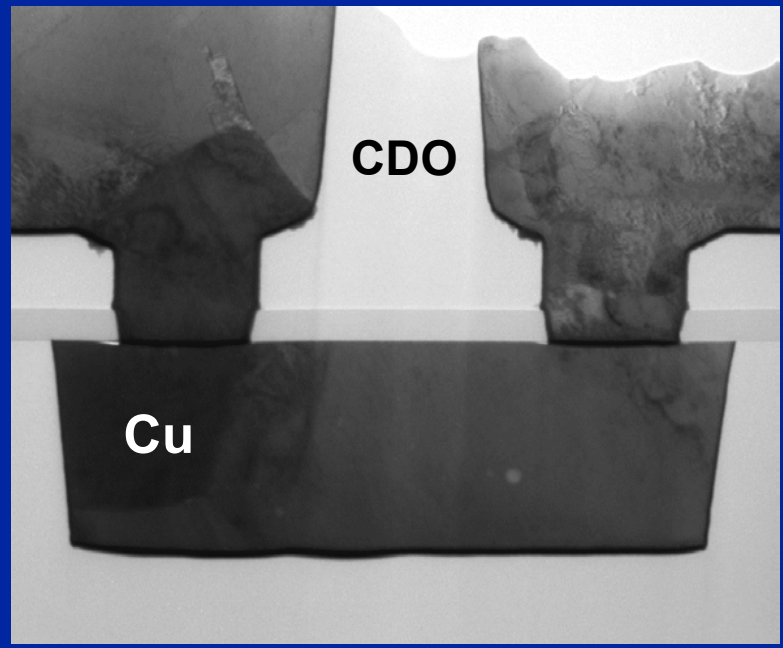


# Electromigration Enabling

Old process

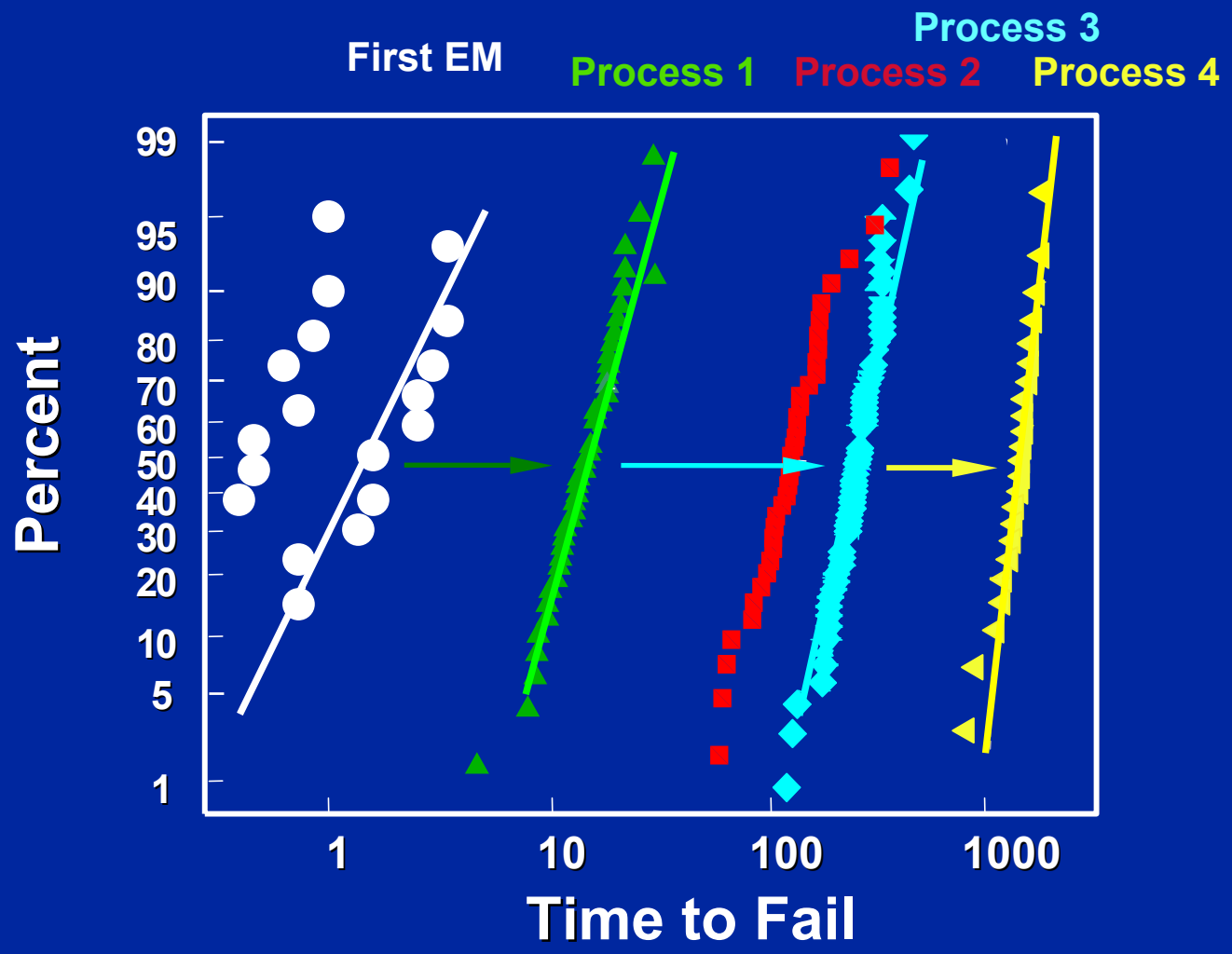



New process




Interface controls EM performance

# Electromigration Improvement



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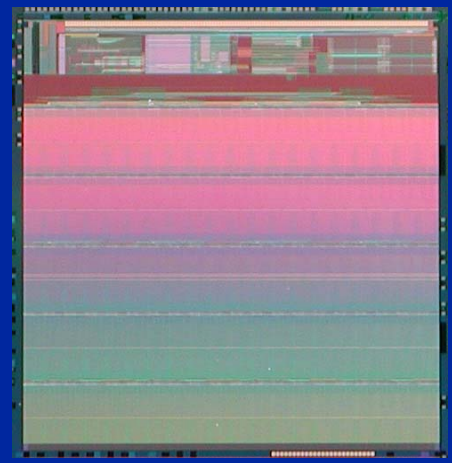
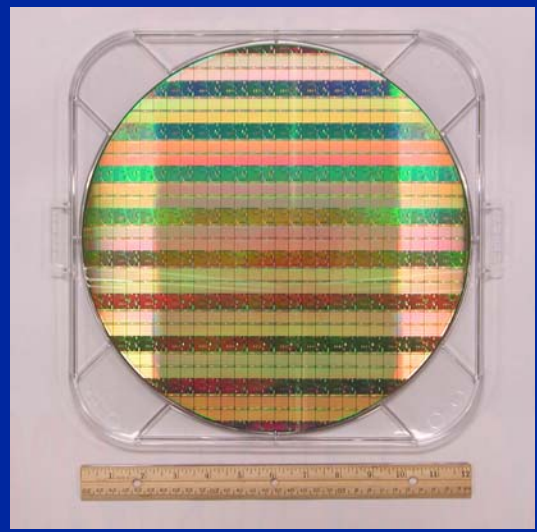
# SRAM Yield Vehicle

- 52 MBit CMOS SRAM
- 330 million transistors in one SRAM die
- 120 billion transistors on one 300 mm wafer

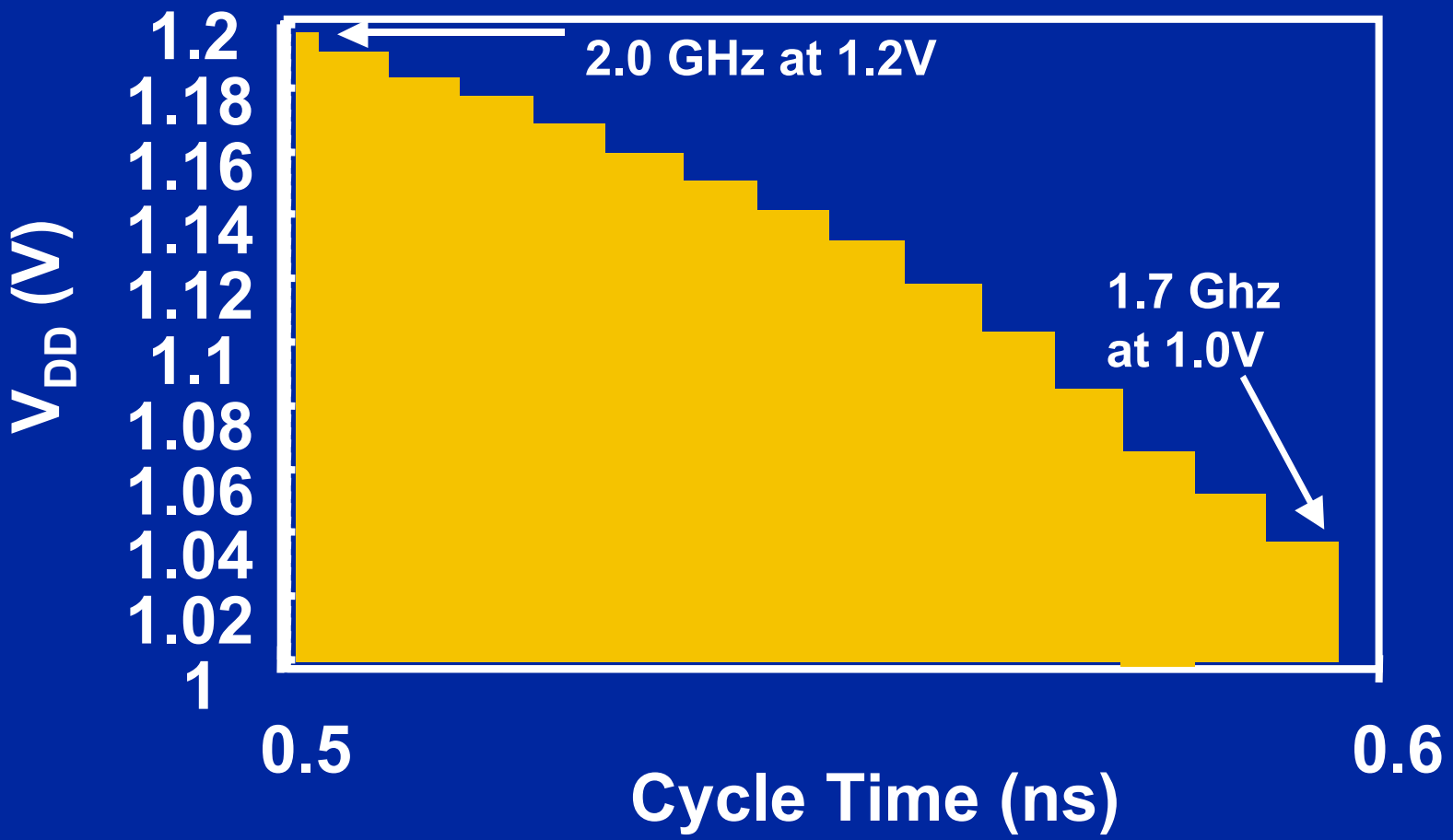
10.1 mm

10.8 mm





# 52MBit SRAM Schmoo Plot



# Conclusions

- 50 nm strained silicon channel transistors
- Strain-enhanced mobility increases saturated drive current by 10 - 20%
- 1 $\mu m^2$ 6-T SRAM at 0.75 V to 1.2 V low voltage operation
- 7 layers of low resistance copper with CDO ILD (k=2.9) for low resistance wiring
- 52M bit SRAM with 330M strain silicon channel transistors

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- Quality and Reliability Engineering
- Technology Computer Aided Design

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